PIC32MZ EMBEDDED CONNECTIVITY (EC)

PIC32MZ Embedded Connectivity (EC) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity (EC) family devices that you have received conform functionally to the current Device Data Sheet (DS60001191**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Embedded Connectivity (EC) family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections (if applicable) start on page 18, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ Embedded Connectivity (EC) family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A3	A4	A5
PIC32MZ1024ECG064	0x05103053	0x3	0x4	0x5
PIC32MZ1024ECH064	0x05108053			
PIC32MZ1024ECM064	0x05130053			
PIC32MZ2048ECG064	0x05104053			
PIC32MZ2048ECH064	0x05109053			
PIC32MZ2048ECM064	0x05131053			
PIC32MZ1024ECG100	0x0510D053			
PIC32MZ1024ECH100	0x05112053			
PIC32MZ1024ECM100	0x0513A053			
PIC32MZ2048ECG100	0x0510E053			
PIC32MZ2048ECH100	0x05113053			
PIC32MZ2048ECM100	0x0513B053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001191**C**) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A3	A4	A5
PIC32MZ1024ECG124	0x05117053	0x3	0x4	0x5
PIC32MZ1024ECH124	0x0511C053			
PIC32MZ1024ECM124	0x05144053			
PIC32MZ2048ECG124	0x05118053			
PIC32MZ2048ECH124	0x0511D053			
PIC32MZ2048ECM124	0x05145053			
PIC32MZ1024ECG144	0x05121053			
PIC32MZ1024ECH144	0x05126053			
PIC32MZ1024ECM144	0x0514E053			
PIC32MZ2048ECG144	0x05122053			
PIC32MZ2048ECH144	0x05127053			
PIC32MZ2048ECM144	0x0514F053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001191**C**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
ADC	INT0 Trigger	1.	When using INT0 as a trigger source for ADC conversion, the INT0EP bit in the INTCON register controls which edge triggers the conversion (rising or falling). However, only a rising edge will trigger the conversion.	X	X	X
ADC	Data Format	2.	Two's complement (signed) input mode does not produce expected results.	X	X	X
Boot Flash	Boot Sequence	3.	When Boot Flash 1 is selected to be mapped to a Lower Boot Alias memory, the device may instead incorrectly map Boot Flash 2.	X	X	X
Comparator Voltage Reference	Range Selection	4.	The Comparator Voltage Reference (CV_{REF}) module range selection (CVRR bit in the CVRCON register) does not function.	X	X	X
Ethernet Controller	Alternate MII and RMII Configurations	5.	The Alternate Ethernet pins, AERXDV and AERXCLK, are not available on 100-pin devices.	X	X	X
Ethernet Controller	MII Configuration	6.	MII mode is not available on 64-pin devices.	X	X	X
Ethernet Controller	RMII Mode	7.	MII pins that are not used by the Ethernet module during RMII operation may not be available for other functions.	X	X	X
I/O Port	Open Drain	8.	The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.	X	X	X
Oscillator	FRC Tuning	9.	Changing values in the OSCTUN register has no effect on the FRC accuracy.	X	X	X
Oscillator	Ceramic Resonator	10.	The Ceramic Resonator cannot be used as an input to the Oscillator module (OSC1/OSC2 pins).	X	X	X
Secondary Oscillator	Crystal Oscillator	11.	A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).	X	X	X
Reserved	—	12.	—	—	—	—
Power-Saving Modes	Dream Mode	13.	Dream mode does not function.	X	X	X
Power-Saving Modes	Sleep Mode	14.	The device may not exit Sleep mode.	X	X	X
SPI	Maximum Speed Operation	15.	The SPI clock speed does not meet the published specification.	X	X	X
Reserved	—	16.	—	—	—	—
System Bus	Permission Access	17.	When Permission Access is enabled, any access by an initiator that is not allowed will not succeed; however, the status registers may not accurately report the violations.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
USB	Suspend Mode	18.	The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.	X	X	X
USB	—	19.	The USB module requires a start-up delay.	X	X	X
USB	Endpoint FIFO	20.	Endpoint FIFOs cannot be read using 32-bit reads.	X	X	X
Reserved	—	21.	—	—	—	—
Watchdog Timer	Window Mode	22.	When the Watchdog Timer is used in Window mode, the module may issue a Reset even if the user tries to clear the module within the allowed window.	X	X	X
Watchdog Timer	Reset Trigger	23.	When the Watchdog Timer expires during Sleep mode, it causes a Reset rather than a non-maskable interrupt (NMI).	X	X	X
PMP	Address Lines	24.	PMP address lines block the use of lower-order functions when the PMP is used but the corresponding bit in the PMAEN register is cleared.	X	X	X
I^2C	Master Stop	25.	The hardware Master Stop control does not function.	X	X	X
Crypto Engine	Byte Ordering	26.	The Crypto Engine processes data in big-endian order rather than little-endian.	X	X	X
Random Number Generator	True Random Number Generator (TRNG) Mode	27.	TRNG mode does not function.	X	X	X
Flash	Code-Protect	28.	Once the Code-Protect feature is enabled, a device cannot be erased using ICSP™ or JTAG.	X		
ADC	Group Interrupt	29.	When using Channel Scan, Class 3 inputs are always part of the Group Interrupt regardless of the setting of the AGIENx bits in the AD1IRQENx register.	X	X	X
SQI	Soft Reset	30.	A Soft Reset is only possible when clock divider values are '0' and '1'.	X	X	X
SQI	XIP Mode	31.	XIP mode is not operational.	X	X	X
SQI	Buffer Thresholds	32.	Transmit and receive operation may not function properly.	X	X	X
SQI	Interrupts	33.	Some Interrupt Signal Enable bits are set upon a Reset.	X	X	X
SQI	Read Clock Speed	34.	Clock for read operations does not meet the published specification.	X	X	X
SQI	Transmit Buffer Empty Status	35.	Upon a reset, the Transmit Buffer Empty Status (TXEMPTYIF) bit in the SQI1INTSTAT register is cleared to zero instead of being set to one.	X	X	X
Comparator	Idle Mode	36.	The Comparator cannot be disabled when the device is in Idle mode.	X	X	X
Comparator	Offset	37.	The Comparator offset does not meet the published specification	X	X	X
I/O Pins	SOSCO Function	38.	I/O pins shared with the SOSCO function cannot be used as general purpose input or output.	X	X	X
I^2C	Overrun Interrupt	39.	A Slave interrupt is not generated during an overrun condition.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
Flash Memory	Program Write Protect	40.	The Program Write Protect (PWP) bits protect all Program Memory.	X	X	X
Oscillator	POSC	41.	A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/OSC2 pins).	X	X	
5V Tolerant I/O Pins	Pull-ups	42.	Internal pull-up resistors may not guarantee a logical '1' on digital inputs on 5V tolerant pins.	X	X	X
ADC	—	43.	Certain ADC operating modes are not supported.	X	X	X
ADC	—	44.	The ADC module does not meet published specifications.	X	X	X
Prefetch	Module Disable	45.	Disabling the Prefetch does not invalidate contents.	X	X	X
Oscillator	Clock Switch	46.	Switching the System Clock (SYSCLK) to the Secondary PLL (SPLL) causes a device Reset. This affects both software and hardware (IESO) clock switching.	X	X	X
DMA	Interrupt Trigger	47.	A UART6 Transfer Done interrupt cannot be used to trigger DMA activity.	X	X	X
UART	Auto-baud	48.	The Automatic Baud Rate feature does not function to set the baud rate.	X	X	X
Deadman Timer	NMI	49.	The Deadman Timer triggers a device Reset instead of a Non-Maskable Interrupt (NMI).	X	X	X
Oscillator	POSC Crystal	50.	Crystal support for the Primary Oscillator does not meet published specifications for frequency and voltage.	X	X	X
Reserved	—	51.	—	—	—	—
I^2C	SDA Hold Time	52.	Lengthening the SDA hold time causes bus collisions in 1 MHz mode.	X	X	X
System Bus	Simultaneous Access	53.	CAN data may become corrupted during simultaneous operation.	X	X	X
Power-Saving Modes	Sleep Mode	54.	The minimum CAN pulse width does not wake the device.	X	X	X
Oscillator	Reference Clock	55.	The Reference Clock cannot use input frequencies greater than 100 MHz.	X	X	X
UART	Synchronization	56.	On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: ADC

When using INT0 as a trigger source for ADC conversion, the INT0EP bit in the INTCON register controls which edge triggers the conversion (rising or falling). However, only a rising edge will trigger the conversion.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

2. Module: ADC

Two's complement (signed) input mode does not produce the expected results. Signed mode selections are SHxMOD<1:0> = 01 for single-ended or SHxMOD<1:0> = 11 for differential inputs.

Work arounds:

Work around 1

Use two's complement format for all inputs. The Two's complement format works properly when all sample and holds are set for this format. Single-ended or Differential mode can still be selected independently. Use one of the following settings for SH0MOD through SH5MOD:

- SHxMOD<1:0> = 01, for signed single-ended

  or

- SHxMOD<1:0> = 11, for signed differential inputs

Work around 2

Use unipolar (unsigned) mode selections for all sample and holds. Where needed, convert the unsigned results to signed values. Unsigned 12-bit results can be converted to signed values by subtracting 2048 from the signed result. Use one of the following settings for SH0MOD through SH5MOD:

- SHxMOD<1:0> = 00, for unsigned single-ended

  or

- SHxMOD<1:0> = 10, for unsigned differential inputs

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

3. Module: Boot Flash

When Boot Flash 1 is selected to be mapped to a Lower Boot Alias memory, the device may instead incorrectly map Boot Flash 2.

Work around

Program an invalid sequence number (such as 0xFFFFFFFF or 0x00000000) into Boot Flash 2. This will force the device to map Boot Flash 1 into the Lower Boot Alias memory.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

4. Module: Comparator Voltage Reference

The Comparator Voltage Reference (CV_{REF}) module range selection (CVRR bit in the CVRCON register) does not function. The default setting of the CV_{REF} Range Selection bit (CVRR) is set to 0 to 0.67 CV_{RSRC}, with a step size of $CV_{RSRC}/24$, and *cannot* be changed.

Work around

Use an External Voltage Reference and adjust it appropriately to achieve the desired CV_{REF} output.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

5. Module: Ethernet Controller

The Alternate Ethernet pins, AERXDV and AERXCLK, are not available on 100-pin devices.

Work around

Only use either the MII or RMII configuration.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

6. Module: Ethernet Controller

MII mode is not available on 64-pin devices. In this mode, the Ethernet pin, ERXD2, is not available.

Work around

Use the RMII or Alternate RMII configurations.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

7. Module: Ethernet Controller

MII pins that are not used by the Ethernet module during RMII operation are not released, and therefore, lower priority functions on these pins are not available in this mode. However, higher priority functions on these pins, such as EBI and analog inputs (for ADC and Comparators), can still be used.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

8. Module: I/O Port

The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

9. Module: Oscillator

Changing values in the OSCTUN register has no effect on the FRC accuracy.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

10. Module: Oscillator

The Ceramic Resonator cannot be used as an input to the Oscillator module (OSC1/OSC2 pins).

Work around

Instead, use either a crystal oscillator or the external clock.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

11. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).

Work around

Instead, use the external clock.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

12. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

13. Module: Power-Saving Modes

Dream mode is intended as a feature allowing DMA operation while the CPU is in Idle mode; however, Dream mode does not function.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

14. Module: Power-Saving Modes

The device may not exit Sleep mode.

Work arounds

Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 configuration register.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

15. Module: SPI

The SPI clock speed does not meet the published specification. The maximum supported SPI clock speed is 27 MHz.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

16. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

17. Module: System Bus

When Permission Access is enabled, any access by an initiator that is not allowed will not succeed; however, the status registers may not accurately report the violations.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

18. Module: USB

The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.

Work around

Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to '0'.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

19. Module: USB

The USB module requires a start-up delay.

Work around

When enabling the USB PLL, add a three second delay before turning on the USB module.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

20. Module: USB

Endpoint FIFOs cannot be read using 32-bit reads.

Work around

Use 8-bit reads, reading each portion and copying into a 32-bit value.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

21. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

22. Module: Watchdog Timer

When the Watchdog Timer is used in Window mode, the module may issue a Reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

23. Module: Watchdog Timer

When the Watchdog Timer expires during Sleep mode, it causes a Reset rather than a Non-maskable Interrupt (NMI).

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

24. Module: PMP

PMP address lines block the use of lower-order functions when the PMP is used but the corresponding bit in the PMAEN register is cleared.

For example, on 100-pin devices, pin 2 is EBIA5/ AN34/PMA5/RA5; however, clearing bit 5 of the PMAEN register does not allow RA5 to function as GPIO even though PMA5 is not to be used with the PMP.

Work around

Higher-order functions are available and should be used instead. As described in the previous example, EBIA5 and AN34 would be available.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

25. Module: I^2C

The hardware Master Stop control (PEN bit) does not function.

Work around

Instead of hardware, use software to create the Stop condition, which involves execution of two separate steps.

Step 1:

During software setup do the following:

1. Clear the LAT bit of the SDA pin.
2. Clear the TRIS bit of the SDA pin to be configured as an output.
3. Set the LAT bit of the SCL pin.
4. Set the TRIS bit of the SCL pin to be configured as an input.
5. Enable the I^2C module by setting the ON bit in the I2CxCON register.
6. To avoid using software delay loops, set up a Timer module with an interval equivalent to 1 BRG time. The Timer interrupt will occur for every 1 BRG time period.

Step 2:

To create the Stop condition on the I^2C bus, *do not* set the PEN bit in the I2CxCON register. Instead, a software routine should be invoked to provide delays and manipulate the GPIO that the I^2C pins share that would create a Stop condition. A Stop condition occurs when SDA goes high 1 BRG time after SCL goes high. SCL goes high at least 1 BRG time after receiving ACK or NACK from the slave.

After software setup, do the following to create the Stop condition:

1. Start the Timer module.
2. After 1 BRG time period has elapsed, disable the I^2C module by clearing the ON bit in the I2CxCON register.
3. After 2 BRG time periods have elapsed, change the direction of the SDA pin to an input by setting the corresponding TRIS bit.
4. After 4 BRG time periods have elapsed, enable the I^2C module by setting the ON bit in the I2CxCON register.
5. Clear the LAT bit of the SDA pin.
6. Clear the TRIS bit of the SDA pin to be configured as an output.
7. Set the LAT bit of the SCL pin.
8. Set the TRIS bit of the SCL pin to be configured as input.
9. Stop the Timer module.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

26. Module: Crypto Engine

The Crypto Engine processes data in big-endian order rather than little-endian.

Work around

Use the SWAPEN bit (CECON<5>) to byte-reverse the data on input. After the data is processed, it must be byte-reversed by software or programmable DMA.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

27. Module: Random Number Generator

True RNG mode does not function.

Work around

Instead, use Pseudo-Random Number Generator (PRNG) mode.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

28. Module: Flash

Under normal conditions, once the Code-Protect feature is enabled, a device cannot be accessed (read and/or write) through external interfaces such as ICSP™ or JTAG. To gain access through these interfaces, the Code-Protect bit must be erased, either by issuing an erase command (using ICSP or JTAG) or with the help of RTSP code. However, the device erase command using ICSP or JTAG does not function, once the Code-Protect feature is enabled.

Work arounds:

Work around 1

Use the RTSP method to update code in a Code-Protect enabled device. In this mode, Flash memory can be erased and programmed with desired data.

Work around 2

Use the RTSP method with the Live-Update feature of the device to erase the Code-Protect bit. Using this method, the application will erase the Code-Protect bit located in the inactive Boot Flash memory, and update this Boot Flash sequence to a higher number versus the active Boot Flash memory. On the next POR, Boot Flash memory with the erased Code-Protect bit will be used to configure the device, including Code-Protect configuration.

Affected Silicon Revisions

A3	A4	A5					
X							

29. Module: ADC

When using Channel Scan, Class 3 inputs are always part of the Group Interrupt regardless of the setting of the AGIENx bits in the AD1IRQENx register. Conversions should only be part of the Group interrupt if a AGIENx bit is set.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

30. Module: SQI

A SQI Soft Reset, which is controlled by the RESET bit in the SQI1CFG register does not work when the CLKDIV<7:0> bits in the SQI1CLKCON register have a value of two or higher.

Work around

Set the CLKDIV<7:0> bits to a value of zero or one.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

31. Module: SQI

XIP mode is not operational (MODE<2:0> bits = `011` in the SQI1CFG register).

Work around

Use PIO mode (MODE<2:0> bits = `001`) or DMA mode (MODE<2:0> bits = `010`).

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

32. Module: SQI

Transmit and receive operation may not function properly.

Work around

Set the TXCMDTHR<5:0> and RXCMDTHR<5:0> bits in the SQI1CMDTHR register to multiples of 4 (32-bit aligned data buffers).

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

33. Module: SQI

The TXEMPTYISE, TXTHRISE, RXEMPTYISE, RXTHRISE, and CONEMPTYISE Interrupt Signal Enable bits in the SQI1INTSEN register are enabled on a device Reset.

Work around

Clear these bits by software.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

34. Module: SQI

Clock speed for read operations does not meet the maximum specification (SQ10) of 50 MHz. For read operations the maximum clock is 25 MHz.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

35. Module: SQI

For all resets, the Transmit Buffer Empty Status (TXEMPTYIF) bit in the SQI1INTSTAT register is cleared to zero instead of being set to one.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

36. Module: Comparator

The SIDL bit in the CMSTAT register is intended to stop all Comparator modules when the CPU enters Idle mode. However, this bit does not function, and all enabled modules will continue to operate.

Work around

Disable the Comparator module by clearing the ON bit in the CMxCON register prior to entering Idle mode.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

37. Module: Comparator

The Input Offset Voltage parameter (D300) is not within the published data sheet specification. The typical value is ±30 mV.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

38. Module: I/O Pins

When the Secondary Oscillator is disabled through the FSOSCEN bit (DEVCFG1<6>), the SOSCO pin does not tri-state and is driven to Vss. An I/O pin shared with the SOSCO function cannot be used as a general purpose input or output.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

39. Module: I^2C

When operating in Slave mode, the I^2C module does not trigger an interrupt when an overrun condition occurs.

Work around

Monitor the I2COV bit in the I2CxSTAT register using software.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

40. Module: Flash Memory

Under normal conditions, setting the Program Write Protect (PWP) bits sets a mark below which the program memory is protected. Memory above this setting may be erased or written. However, the device protects all of program memory when any PWP bits are set.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

41. Module: Oscillator

Depending on the revision of silicon, a crystal oscillator cannot be used as the input to the Primary Oscillator (OSC1/OSC2 pins).

Work around

For Revision A3 and A4 silicon:

Use an external clock or an internal FRC.

For Revision A5 silicon:

See Data Sheet Clarification 3: Primary Oscillator.

Affected Silicon Revisions

A3	A4	A5					
X	X						

42. Module: 5V Tolerant I/O Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load doesn't exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

43. Module: ADC

Note: A related code example is available in MPLAB Harmony, Version 1.02 or later. For more information, visit http://www.micochip.com/harmony.

The following ADC operating modes are not supported:

- Software polling of ADC status bits
- Manual software ADC triggering
- ADC interrupt modes (use DMA Interrupt mode)
- ADC SFR accesses by the CPU while ADC is operating
- ADC Boost or low-power mode.
- Individual ADC Input Conversion Requests (i.e., RQCNVRT bit in the ADCCON3 register)
- Use of ADC S&H Channels 0-4 except for calibration
- Any ADC references other than external V_{REF+} and V_{REF-} pins
- ADC Differential mode

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

44. Module: ADC

For Revision A3 and A4 silicon:

> **Note:** A related code example is available in MPLAB Harmony, Versions 1.00 or 1.01. These versions are available in the MPLAB Harmony archive. For more information, visit http://www.micochip.com/harmony.

The ADC module does not meet the published Throughput Rate (AD51) and Full-Scale Input Range (AD12) specifications. The updated Maximum Throughput Rate (AD51) specification is 125 ksps, assuming 16x Oversampling mode. The updated Maximum Full-Scale Input Range is 2.5V for both Differential and Singled-Ended modes. The updated Minimum Full-Scale Input Range is -2.5V for Differential mode.

For Revision A5 silicon with date codes of 1503xxx (i.e., 1/12/15) or later:

> **Note:** A related code example is available in MPLAB Harmony, Version 1.02 or later. For more information, visit http://www.micochip.com/harmony.

These devices will have ADC performance as specified in Table 3 and Table 4.

For Revision A5 silicon with date codes prior to 1503xxx (i.e., 1/12/15):

These devices were not calibrated appropriately and may not perform to the specifications defined in Table 3 and Table 4.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

TABLE 3: ADC1 MODULE SPECIFICATIONS

AC CHARACTERISTICS(3,4)			Standard Operating Conditions (see Notes 2,3,4): 2.5V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +85°C				
Param.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	VREFH = VREF+ (**Note 1**)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(**Note 1**)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	—
AD08 AD08a	IREF	Current Drain	— —	100 .002	150 1	µA µA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Range	0	—	Lesser of VDD – 0.6 or 2.5	V	Single-ended mode only (Differential mode is not supported)
AD14	VINCM	Common Mode Input Voltage	AVSS + VREF/2	—	AVDD – VREF/2	V	—
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	≤ 10k	Ω	(**Note 1**) For minimum sampling time

Note 1: These parameters are not characterized or tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

3: Specifications are based on adherence to the requirements listed in **Section 28.1 "ADC Configuration Requirements"**.

4: All data was collected using a dedicated external precision voltage source connected to VREF+ and with VREF- tied to external AVSS. External VREF+ and VREF- must be used at all times.

TABLE 3: ADC1 MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS(3,4)			Standard Operating Conditions (see Notes 2,3,4): 2.5V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +85°C				
Param.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	8 data bits			bits	—
AD21c	INL	Integral Nonlinearity	-5	±3	+5	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD22c	DNL	Differential Nonlinearity	-1	±1	+2	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD23c	GERR	Gain Error	-10	±3	+10	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD24c	EOFF	Offset Error	-9	±1	+9	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD25e	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	42	—	dB	—
AD34b	ENOB	Effective Number of bits	—	7	—	bits	—

Note 1: These parameters are not characterized or tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

3: Specifications are based on adherence to the requirements listed in **Section 28.1 "ADC Configuration Requirements"**.

4: All data was collected using a dedicated external precision voltage source connected to VREF+ and with VREF- tied to external AVSS. External VREF+ and VREF- must be used at all times.

TABLE 4: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS[2,4,5]			Standard Operating Conditions (see Notes 3,4,5): 2.5V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +85°C				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.[1]**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	1000	—	2000	ns	—
Throughput Rate							
AD51	FTP	SH0 – SH4 (Class 1 Inputs)	—	—	—	—	SH0-SH4 functionality is not supported. Sampling must be performed on SH5 only. See **Note 3**.
		SH5 (Class 2 and 3 Inputs)	—	—	66.6	ksps	Single Class 2 or 3 input, 1 MHz ADC Clock, Source impedance ≤ 10 kΩ, SAMC = 'b00001010, Assumes there are no pending sample conversion operations at time of trigger. See **Note 3**.
		Conversion Pipeline	—	—	1	Msps	—
Timing Parameters							
AD60	TSAMP	Sample Time for SH0-SH4 (Class 1 Inputs)	—	—	—	TAD	SH0-SH4 functionality is not supported. Sampling must be performed on SH5 only.
		Sample Time for SH5 (Class 2 and 3 Inputs)	10	—	—	TAD	Source Impedance ≤ 10 kΩ, 1 MHz ADC clock
AD62	TCONV	Conversion Time (after sample time is complete)	—	—	10	TAD	SH0-SH4 functionality is not supported. Sampling must be performed on SH5 only. For SH5, TSAMP + TCONV provides Trigger to data ready timing;
AD64	TCAL	Calibration Time	—	160	—	TAD	—
AD65	TWAKE	Wake-up time from Low-Power Mode	—	2	—	TAD	—

Note 1: These parameters are not characterized, or tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

3: Assuming correct PLL configuration (i.e., 192 MHz system clock).

4: Specifications are based on adherence to the requirements listed in **Section 28.1 "ADC Configuration Requirements"**.

5: All data was collected using a dedicated external precision voltage source connected to VREF+ and with VREF- tied to external AVSS. External VREF+ and VREF- must be used at all times.

45. Module: Prefetch

The Prefetch module does not invalidate buffer contents when the module is disabled by setting the PREFEN<1:0> bits to 'b00.

Work around

To disable the Prefetch module, execute four 32-bit NOP commands before and after setting the PREFEN<1:0> bits to 'b00.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

46. Module: Oscillator

Switching the System Clock (SYSCLK) to the System PLL (SPLL) causes a device Reset. This affects both software and hardware (IESO) clock switching.

Work around

To switch the clock source, disable IESO, and execute the following steps in software:

1. Reduce the speed of all peripheral buses to 128:1 through PBCLKx (where 'x' ≠ 7) and reduce the speed of the CPU bus to 128:1 through PBCLK7.
2. Perform the clock switch.
3. Set the speed of the CPU bus to the previous clock switch divisor and set the speed of the peripheral buses to their previous clock switch divisor.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

47. Module: DMA

The UART6 Transfer Done Interrupt (190) cannot be used to trigger a DMA activity, such as a start or a stop.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

48. Module: UART

The UART Automatic baud rate feature is intended to set the baud rate during run-time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

49. Module: Deadman Timer

The Deadman Timer should trigger a Non-Maskable Interrupt (NMI) when the timer runs out or when an incorrect value is written to the DMTPRECLR or DMTCLR registers. Instead, the Deadman Timer triggers a device Reset without a NMI.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

50. Module: Oscillator

The Primary Oscillator does not meet the published specifications for crystal support.

Work around

To use a crystal with the Primary Oscillator, the following limitations on voltage and frequency must be observed:

- $2.4V \leq V_{DD} \leq 3.6V$
- 4 MHz ≤ Crystal Speed ≤ 12 MHz

Additional details can be found in Data Sheet Clarification 3: Primary Oscillator.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

51. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

52. Module: I²C

Setting the SDAHT bit in the I²C module lengthens the time that the SDAx pin is held after SCLx falls to 300 ns from 100 ns. However, the actual hold time is longer than 300 ns, and as a result, it causes a bus collision when operating at 1 MHz.

Work around

Do not set the SDAHT bit when operating the I²C module at 1 MHz.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

53. Module: System Bus

When operating the system bus at 8 MHz, having the CAN module access one RAM bank while the Crypto module accesses the other RAM bank can cause the CAN data to become corrupted.

Work around

Operate the system bus at frequencies faster than 8 MHz.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

54. Module: Power-Saving Modes

The CAN module can wake the processor from Sleep mode. However, if the bus line filter is enabled through the WAKFIL bit (CiCFG<22>), and the operating pulse width is 560 ns or less, the CAN module does not wake the device.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

55. Module: Oscillator

The Reference Module cannot accept input frequencies greater than 100 MHz. Therefore, SYSCLK cannot be used as an input if the SYSCLK operates at frequencies greater than 100 MHz.

Work around

Instead of using SYSCLK, use PBCLK1 as the input, which is limited to 100 MHz and is synchronized to SYSCLK.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

56. Module: UART

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement a ACK/NAK software handshake protocol to repeat lost packet transfers after restoring UART synchronization.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001191**C**):

Note:	Corrections in tables are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: ADC Configuration Requirements

Note:	A related code example is available in the latest release of MPLAB Harmony. For more information, visit: http://www.micochip.com/harmony.

To meet ADC specifications, the following steps must be performed:

1. Set the ADC Configuration words, as follows:

```
AD1CAL1 = 0xB3341210;
AD1CAL2 = 0x01FFA769;
AD1CAL3 = 0x0BBBBBB8;
AD1CAL4 = 0x000004AC;
AD1CAL5 = 0x02028002;
```

2. Perform self-calibration. The input mode for SH0-SH5 must be set to the unipolar differential input mode by setting the SHxMOD<1:0> bits (AD1MOD<1:0>) = `10`.

Note:	SH0 through SH4 functionality and ADC Differential mode are not supported; however, both are required for auto-calibration. Sampling must be performed on SH5 only.

In addition, the following restrictions apply:

Supported ADC operating modes:

- Scan mode only with DMA interrupt
- The maximum number of used ANx inputs are limited by the available DMA channels (maximum of eight)
- The first (8) conversion after enabling the ADC must be discarded
- ADC Single-ended mode only
- The ADC Clock, TAD, must be limited to 500 kHz ≤ TAD ≤ 1 MHz (i.e., 2 µs ≤ TAD ≤ 1 µs).
- HDW Oversampling is supported, but it is not required, and will not impair accuracy; however, it will reduce the ADC ANx input throughput by the oversample ratio in use
- ANx VIN maximum is limited to ≤ 2.5V
- VREF+ ≤ VDD = AVDD ≥ 2.5V
- Use of external VREF+ and VREF- pins only for ADC reference (VREFSEL<2:0> bits are equal to `'b011`):
  - VREF- = Can be connected to AVSS externally, but not internally
  - VREF+ can be connected to AVDD externally if required, but not internally

Unsupported ADC operating modes:

- Software polling of ADC status bits
- Manual software ADC triggering
- ADC interrupt modes (use DMA Interrupt mode)
- ADC SFR accesses by the CPU while ADC is operating
- ADC Boost or low-power mode.
- Individual ADC Input Conversion Requests (i.e., RQCNVRT bit in the ADCCON3 register)
- Use of ADC S&H Channels 0-4 except for calibration
- Any ADC references other than external VREF+ and VREF- pins
- ADC Differential mode

2. Module: I/O Ports

The injection current for certain I/O pins is higher than specified in the data sheet. The injection current for the pins in **bold** type are listed in the following table.

TABLE 37-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
DI50	IIL	Input Leakage Current (Note 3)					
		I/O Ports (with the following three exceptions)	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
		SOSCI/RPC13/RC13	**—**	**—**	**±500**	**μA**	**VSS ≤ VPIN ≤ VDD, Pin at high-impedance**
		SOSCO/RPC14/TI1CK/RC14	**—**	**—**	**±500**	**μA**	**VSS ≤ VPIN ≤ VDD, Pin at high-impedance**
		RPF3/USBID/RF3	**—**	**—**	**±500**	**μA**	**VSS ≤ VPIN ≤ VDD, Pin at high-impedance**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

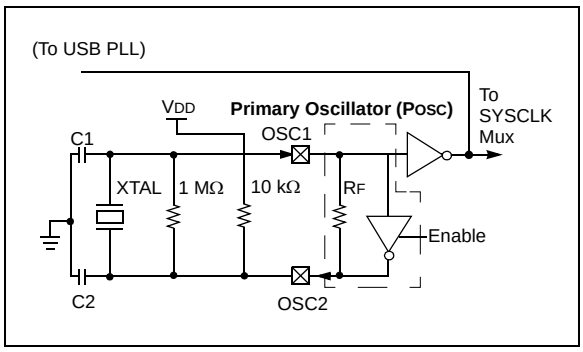
3: Negative current is defined as current sourced by the pin.

3. Module: Primary Oscillator

The Primary Oscillator logic in **Figure 8-1: "PIC32MZ EC Family Oscillator Block Diagram"** of the current device data sheet omitted a pull-up resistor (R_K), which is necessary to ensure stable start-up of the Primary Oscillator when it is running from a crystal. This resistor must be 10 kΩ and connected between OSC2 and V_{DD}.

The following figure shows the amended portion of the diagram.

FIGURE 8-1: PIC32MZ EC FAMILY OSCILLATOR BLOCK DIAGRAM



Crystals with a speed of 4 MHz to 12 MHz that meet the following requirements will meet the PIC32MZ oscillation requirements when configured as depicted in Figure 8-1.

1. Manufacturer Drive Level (min) < 10 µW (hard requirements, 1 µW preferred).
2. Manufacturer ESR ≤ 50Ω (hard requirement, lower is better).

How to Calculate XTAL Capacitive loading:

1. PIC32 C_{IN} = C_{OUT} = ~4 pF (PIC32 OSCI and OSCO package pin capacitance).
2. $C1_{MFG}$ = $C2_{MFG}$ = Manufacturer Recommended Load Capacitance.
3. C_{LOAD} = {([C_{IN} + $C1_{MFG}$] [$C2_{MFG}$ + C_{OUT}]) / [C_{IN} + $C1_{MFG}$ + $C2_{MFG}$ + C_{OUT}]} + estimated PCB stray capacitance (2.5 pF)

   (Simplified) C_{LOAD} = (((C_{IN} + $C1_{MFG}$) / 2) + 2.5 pF).

Actual C1, C2 Load value to use:

- C2 = C_{LOAD}
- C1 = (C_{LOAD} - 2 pF)

Validated Crystals

Temperature Range: (-20ºC to +70ºC)

V_{DD} = 2.4V to 3.6V, R_P = 1 MOhm, R_K = 10 kOhm

- TXC 9B-8.000MAAJ-B, (8 Hz throughhole)
- TXC 9B-12.000MEEJ-B, (12 MHz throughhole)
- TXC 7M-12.000MAAE-T, (12 MHz surface mount)

Temperature Range: (-45ºC to +110ºC)

V_{DD} = 2.4V to 3.6V, R_P = 1 MOhm, R_K = 10 kOhm

- ABLS-12.000MHz-L4Q-T, (12 MHz surface mount)

4. Module: Internal FRC Oscillator

Certain specifications were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 37-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	**-5**	**±0.9**	**+5**	**%**	**-40°C ≤ TA ≤ +105°C**

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

5. Module: Internal LPRC Oscillator

Certain specifications were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 37-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal LPRC @ 32.768 kHz(1)						
F21	LPRC	**-8**	**±5**	**+8**	%	0°C ≤ TA ≤ +85°C
		-20	**—**	+20	%	**-40°C ≤ TA < 0°C**

Note 1: Change of LPRC frequency as VDD changes.

APPENDIX A: REVISION HISTORY

Rev A Document (11/2013)

Initial release of this document, issued for revision A3 silicon.

This version includes the following issues: 1 (ADC), 2 (ADC), 3 (Boot Flash), 4 (Comparator Voltage Reference), 5 (Ethernet Controller), 6 (Ethernet Controller), 7 (Ethernet Controller), 8 (I/O Port), 9 (Oscillator), 10 (Oscillator), 11 (Secondary Oscillator), 12 (LPRC Oscillator), 13 (Power-Saving Modes), 14 (Power-Saving Modes), 15 (SPI), 16 (SQI), 17 (System Bus), 18 (USB), 19 (USB), 20 (USB), 21 (USB), 22 (Watchdog Timer), 23 (Watchdog Timer), 24 (PMP), 25 (I^2C), 26 (Crypto Engine), and 27 (Random Number Generator).

Rev B Document (12/2013)

Updated issues 7 (Ethernet Controller) and 14 (Power-Saving Modes).

Content in issue 21, which was included in a previous errata version, was removed and this issue has been marked as **Reserved**.

Added data sheet clarification issues 1 (Power-Down Current) and 2 (Operating Conditions), and silicon issues 28 (Flash) and 29 (ADC).

Rev C Document (4/2014)

Updated for revision A4 silicon.

Content in issues 12 and 16, which was included in a previous errata version, was removed and these issues have been marked as **Reserved**.

Added silicon issues 30 (SQI), 31 (SQI), 32 (SQI), 33 (SQI), 34 (SQI), 35 (SQI), 36 (Comparator), 37 (Comparator), 38 (I/O Pins), 39 (I^2C), 40 (Flash Memory), 41 (Oscillator), 42 (5V Tolerant I/O Pins), 43 (ADC), 44 (ADC), and 45 (Prefetch).

Added data sheet clarification issues 3 (Internal FRC Accuracy), 4 (Internal LPRC Accuracy), 5 (Internal Backup FRC (BFRC) Accuracy), 6 (ADC1 Module Specifications and Timing Requirements), 7 (ADC Configuration Requirements), 8 (SQI Timing Requirements), 9 (DC Temperature and Voltage Specifications.), 10 (Recommended Minimum Connection), and 11 (I/O Ports).

Rev D Document (5/2014)

Updated silicon issues 43 (ADC) and 44 (ADC) and data sheet clarifications 6 (ADC1 Module Specifications and Timing Requirements) and 7 (ADC Configuration Requirements).

Rev E Document (9/2014)

Updated for revision A5 silicon.

Updated silicon issues 24 (PMP), 25 (I^2C), and 41 (Oscillator).

Added silicon issues 46 (Oscillator), 47 (DMA), 48 (UART), 49 (Deadman Timer), 50 (Oscillator), and 51 (Reserved).

Removed data sheet clarifications 1 through 6 and 8 through 11. Issue 7 was retained, which is now issue 1 (ADC Configuration Requirements).

Added data sheet clarifications 2 (I/O Ports) and 3 (Primary Oscillator).

Rev F Document (10/2014)

Content in issue 51, which was included in the previous errata version, was removed and this issue have been marked as **Reserved**.

Updated issue 44 (ADC).

Added data sheet clarification 4 (Internal FRC Oscillator).

Rev G Document (12/2014)

Updated silicon issues 25 (I^2C), 30 (SQI), 43 (ADC), 44 (ADC), and 50 (Oscillator).

Updated Data Sheet Clarification 1 (ADC Configuration Requirements) and 3 (Primary Oscillator).

Added silicon issues 52 (I^2C), 53 (System Bus), 54 (Power-Saving Modes), 55 (Oscillator), and 56 (UART).

Added Data Sheet Clarification 5 (Internal LPRC Oscillator).

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